REMARKS

Claims 1-14 were examined and reported in the Office Action. Claims 1-12 are allowed. Claims 13-14 are rejected. Claims 13-14 are amended. Claims 1-14 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. In The Drawings

It is asserted in the Office Action that Fig. 4 is objected to for containing a foreign language. Applicant has amended Fig. 4 and submits the replacement sheet to overcome the objection. Approval is respectfully requested.

II. 35 U.S.C. § 102(e)

It is asserted in the Office Action that claims 13 and 14 are rejected under 35 U.S.C. § 102(e), as being anticipated by U. S. Patent No. 6,661,714 issued to Lee ("Lee"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131, [a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Applicant's amended claim 13 contains the limitations of "[a] semiconductor memory device comprising: a sense amplifier array unit including a plurality of bit-line sense amplifiers arrayed to each other; a driver, located at one side of the sense amplifier array unit, for generating a driving voltage of the plurality of bit-line sense

amplifiers; a first power line connected to an output node of the driver for supplying the driving voltage to each input node of the plurality of bit-line sense amplifiers is attached in parallel; and a second power line, connected to the first power line in parallel at the output node of the driver, and strapped with the first power line at least one point."

Applicant's amended claim 14 contains the limitations of "[a] semiconductor memory device comprising: a sense amplifier array unit including a plurality of bit-line sense amplifiers arrayed to each other, wherein each bit-line sense amplifier has a first driving voltage input node being a pull-up source and a second driving voltage input node being a pull-down source of bit lines; a driver, located at one side of the sense amplifier array unit, for generating a first and a second driving voltage of the plurality of bit-line sense amplifiers; a first power line connected to a first driving voltage output node of the driver for supplying the first driving voltage to a first input node of each of the plurality of bit-line sense amplifiers is attached in parallel; a second power line, connected to the driving voltage output node of the driver, and strapped with the first power line at least one point; a third power line, which is connected to a second driving voltage output node of the driver for supplying the second driving voltage to a second input node of said each of the plurality of bit-line sense amplifiers is attached in parallel; and a fourth power line, connected to the second driving voltage output node of the driver, and strapped with the third power line at least one point."

It is asserted in the Office Action that Lee discloses LAPG and LA (see Lee, Figs. 4 and 5) are corresponding to the first and second power lines of Applicant's claimed invention. However, LAPG is for controlling a driver SW1 coupled to a supply voltage Varray, not for supplying the supply voltage Varray to each sense amplifier. That is, throughout the LAPG, a control signal generated from a control signal generation circuit 47 is transmitted. Therefore, the LAPG cannot be considered as one of first and second power lines connected to an output node of the driver for delivering or transmitting a driving voltage. Thus, Lee does not teach, disclose or suggest the limitations contained in claim 13 of "a first power line connected to an output node of the driver for supplying the driving voltage to each input node of the plurality of bit-line sense amplifiers is attached in parallel" nor the

limitations contained in claim 14 of "a first power line connected to a first driving voltage output node of the driver for supplying the first driving voltage to a first input node of each of the plurality of bit-line sense amplifiers is attached in parallel;... a third power line, which is connected to a second driving voltage output node of the driver for supplying the second driving voltage to a second input node of said each of the plurality of bit-line sense amplifiers is attached in parallel..."

Therefore, since Lee does not disclose, teach or suggest all of Applicant's amended claims 13 and 14 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(e) has not been adequately set forth relative to Lee. Thus, Applicant's amended claims 13 and 14 are not anticipated by Lee.

Accordingly, withdrawal of the 35 U.S.C. § 102(e) rejections for claims 13 and 14 are respectfully requested.

III. Allowable Subject Matter

Applicant notes with appreciation the Examiner's assertion that claims 1-12 are allowed.

Applicant respectfully asserts that claims 1-14, as they now stand, are allowable for the reasons given above.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-14 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: July 5, 2005

By: _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on July 5, 2005.

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Jean Svoboda